REMARKS

After entry of this amendment, claims 7-9, 11-20 and 26-32 are pending in the application., claim 10 having been canceled and claim 32 having been added. Of the remaining claims 7, 11-13 and 26 have been amended. The amendments are fully supported by the specification, drawings and claims as originally filed. No new matter is added and entry of the amendments is respectfully requested.

In particular, amendments to claims 7, 13 and 26 and added claim 32 are supported, inter alia, by the specification at paragraphs 41, 55 and 101, and by FIGs. 3A, 3B, 5, 15A and 15B, as originally filed.

I. REJECTION OF THE CLAIMS UNDER 102

The Examiner rejected claims 7-11 and 26-30 under 35 U.S.C. 102 as being unpatentable U.S. Patent 4,939,559 to DiMaria et al., hereinafter DIMARIA.

To establish a prima facie case of anticipation it must be established that each and every element set forth in the claim is found, either expressly or inherently, in a single prior art reference. M.P.E.P. §2131. Moreover, the reference must be enabling and describe the claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the art. In re Paulsen, 31 USPQ2d 1671 (Fed. Cir. 1994).

The Examiner suggests that DIMARIA anticipates the claimed invention by disclosing in FIG. 1 and at column 7, lines 39-51:

a gate electrode **2** made of a diffusive metal (i.e., silver);

a floating gate **4**;

source **6**, drain **7** and channel regions all part of a continuous semiconductor material **8** and said source/drain regions are doped regions;

a gate insulator 5 extending between said floating gate and said channel and said gate electrode, said gate insulator having conductive paths (depicted by arrows) and portions of the diffusive metal (shaded area).

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

DIMARIA is directed to a memory device having dual electron injectors, and a "off-stoichiometry" insulator, i.e., a silicon-rich, silicon dioxide (SiO_2) insulator between the injectors. The insulator layer between the injectors is rendered conductive during deposition through the addition of an excess of silicon or a metallic specie. The resulting conductive insulator provides a means for draining off trapped charge in the insulator resulting in a device capable of from 10^8 to greater than 10^{10} write-erase cycles before threshold collapse occurs. (Abstract).

In contrast, the present invention is directed to a thin film transistor memory device or cell fabricated using low temperature oxides on inexpensive glass or plastic substrates. Low temperature oxides are used because of the low melt temperature of the glass or plastic substrate. The memory cells include a floating gate separated from a gate electrode portion of a gate line by an insulator formed from the low temperature oxide. The gate electrode portion includes a diffusive conductor that diffuses through the insulator under the application of a write voltage to form a conductive path, CP, through the insulator that couples the gate line to the floating gate. The floating gate is adapted to act as a diffusion barrier to prevent the

diffused metal from the gate electrode from diffusing into the gate insulator layer below the floating gate. (Abstract and paragraphs 3, 4 and 55).

DIMARIA does not teach the use of a low temperature oxide, a conductive path formed by diffusive conductor or a diffusion barrier. Thus, Applicants respectfully disagree with the rejection.

__Claim 7__

In particular, claim 7 as amended includes the limitation of a gate insulator including a first gate insulator layer disposed between the at least one floating gate and the diffusive metal, and a second gate insulator layer disposed below and coupled to the first gate insulator layer, and "wherein *the first gate insulator layer includes a conductive path formed by the diffusion of conductive elements from the diffusive metal through the gate insulator in response to a write voltage applied to the diffusive metal*, and the *at least one floating gate adapted to prevent the conductive elements from the diffusive metal from diffusing into the second gate insulator layer*".

Applicants submit that the cited reference does not disclose a gate insulator comprising a conductive path formed by the diffusion of conductive elements from the diffusive metal through the gate insulator in response to a write voltage applied to the diffusive metal. Applicants submit that the arrows in insulator **5** extending between electron in injectors 1 and 3 in FIG. 1 of DIMARIA illustrates the injection of electrons from the injectors 1, 3, for negative and positive Vg respectively, and not, as in the present invention, a conductive path formed by the diffusion of conductive elements from a diffusive metal in the gate 2 through the gate insulator. Column 6, lines 49-56 of DIMARIA provides:

> Writing is performed by applying a negative voltage V_g^- to control gate 2 which injects electrons from the silicon-rich silicon dioxide injector or layer 1 into the intervening oxide layer 5 which then flow in the electric field to the floating polysilicon gate 4. Erasing is performed by applying a positive voltage V_g^+ to control gate 2 which injects electrons from the bottom silicon-rich silicon dioxide injector 3 back to control gate 2.

Applicants submit the opposing arrows in FIG. 1 of DIMARIA would be understood by one skilled in the art as showing the injection of electrons under write and erase cycles, rather than a conductive path formed by the diffusion of conductive elements from a diffusive metal through the gate insulator. Thus, Applicants respectfully submit that the above limitation of a conductive path is not disclosed or set forth in the cited reference.

Moreover, contrary to the present invention, DIMARIA discloses that the dual injectors 1, 3, and the insulator 5 disposed between these injectors are rendered conductive during deposition. (Column 5, lines 8-31 of DIMARIA) Thus, Applicants submit that DIMARIA would not be understood by one skilled in the art as disclosing formation of a conductive path by the diffusion of conductive elements from a diffusive metal through the gate insulator after deposition of the insulator and in response to a write voltage applied to the diffusive metal.

Similarly, Applicants submit that DIMARIA would not be understood by one skilled in the art as disclosing or setting forth the limitation of the floating gate being adapted to prevent the conductive elements from the diffusive metal from diffusing into the second gate insulator layer. First, as noted above DIMARIA does not disclose or set forth diffusion of conducting elements from the gate electrode 2, therefore there would be no reason for DIMARIA to disclose or set forth a diffusion barrier. Second, the floating gate is adapted to prevent the

conductive elements from the diffusive metal through the selection of material of the floating gate and the size of the floating gate relative to the diffusive metal. As provided in added claim 32 and noted in the specification, the floating gate comprises a metal selected from the group consisting of W, Al, Cr, TiW, and Cu. As shown in FIGs. 3A, 3B, 5, 15A and 15B the floating gate comprises a width greater than the diffusive metal.

In contrast, DIMARIA at no point discloses or sets forth that the floating polysilicon gate 4 could be made of anything other than polysilicon, and clearly shows the floating polysilicon gate as being equal in size with the gate electrode 2.

Accordingly, Applicants submit that DIMARIA does not disclose or set forth every element in claim 7 as amended, and respectfully requests the rejection be withdrawn, and that claim 7 and claims 8-12, 32 and 33 which are dependent therefrom be allowed.

Claim 26

With regard to independent claim 26, as amended claim 26 includes limitations similar to those of claim 7 as amended, namely, claim 26 includes the limitation of the gate insulator comprises *a conductive path formed from conductive elements from the diffusive metal diffused through the gate insulator in response to a write voltage applied to the diffusive metal.* Thus, Applicants submit claim 26 patentable over DIMARIA for at least the reasons given above with respect to claim 7 for this limitation.

Applicant also submits that claim 26 includes further limitations not disclosed or set forth in DIMARIA and are therefore are patentable over DIMARIA. In particular, added claim 26 includes the limitation that, *the gate insulator comprises a low temperature oxide.*

Applicants respectfully submit that DIMARIA would not be understood by one skilled in the art as disclosing or setting forth the limitation of a gate insulator comprising a low temperature oxide. DIMARIA discloses at column 5, lines 8-63, the formation of the device using conventional, high temperature processes, including oxide growth processes at temperatures of 1,000°C and anneals at temperatures of from 700°C to 1,000°C. Moreover, at no point does DIMARIA disclose or set forth substrates having a low melting temperature, such as glass or plastic, or indeed substrates made of any other material than silicon, therefore there would be no need for DIMARIA to disclose or set forth a gate insulator comprising a low temperature oxide.

Thus, Applicants submit that DIMARIA would not be understood by one skilled in the art as disclosing or setting forth the limitation of a gate insulator comprising a low temperature oxide.

Accordingly, Applicants submit that DIMARIA does not disclose or set forth every element in claim 26 as amended, and respectfully requests the rejection be withdrawn, and that claim 26 and claims 27-31 which are dependent therefrom be allowed.

II. REJECTION OF THE CLAIMS UNDER 103

The Examiner rejected claims 12-20 under 35 U.S.C. 103(a) as being unpatentable over DIMARIA in view of U.S. Patent 5,644,528 to Kojima et al., hereinafter KOJIMA, U.S. Patent 6,005,270 to Noguchi, hereinafter NOGUCHI and/or U.S. Patent 6,420,752 to Ngo et al., hereinafter NGO.

Applicant respectfully traverses this rejection and submits that the amended claims are patentable over the cited references.

Under the Graham test, three factors must be evaluated: the scope and content of the prior art; the differences between the prior art and the claimed invention; and the level of ordinary skill in the art. (MPEP 706). Moreover, to establish a prima facie case of obviousness under 35 U.S.C.§103, three basic criteria must be met: (1) the prior art must provide one of ordinary skill with a suggestion or motivation to modify or combine the teachings of the references relied upon by the Examiner to arrive at the claimed invention; (2) the prior art must provide one of ordinary skill with a reasonable expectation of success; and (3) the prior art, either alone or in combination, must teach or suggest each and every limitation of the rejected claims. The teaching or suggestion to make the claimed invention, as well as the reasonable expectation of success, must come from the prior art, not Applicant's disclosure. In re Vaeck, 20 USPQ2d 1438 (Fed. Cir. 1991); M.P.E.P. §706.02(j).

The Invention:

The invention is directed to a thin film transistor memory device or cell fabricated using low temperature oxides on inexpensive glass or plastic substrates. Low temperature oxides are used because of the low melt temperature of the glass or plastic substrate. The memory cells include a floating gate separated from a gate electrode portion of a gate line by an insulator formed from the low temperature oxide. The gate electrode portion includes a diffusive conductor that diffuses through the insulator under the application of a write voltage to form a conductive path, CP, through the insulator that couples the gate line to the floating gate. The floating gate is adapted to act as a diffusion barrier to prevent the diffused metal from the gate electrode from diffusing into the gate insulator layer below the floating gate

<u>The Prior Art:</u>

As noted above, DIMARIA is directed to a memory device having dual electron injectors, and a "off-stoichiometry" insulator, i.e., a silicon-rich, silicon dioxide (SiO_2) insulator between the injectors. The insulator layer between the injectors is rendered conductive during deposition through the addition of an excess of silicon or a metallic specie. The resulting conductive insulator provides a means for draining off trapped charge in the insulator resulting in a device capable of from 10^8 to greater than 10^{10} write-erase cycles before threshold collapse occurs.

KOJIMA is directed to a transistor memory device having multiple floating gages capable of storing multiple bits of data.

NOGUCHI is directed to a thin film transistor memory device having charge storing layers, made using a glass or plastic substrate.

NGO is directed to a semiconductor device with self-aligned contacts. NGO illustrates and describes a method for making word line structures 210 comprising multiple layers including a polysilicon layer 218 and 226 separated by a silicide layer 224 that serves as a cap layer for the stacked gate structure 210. (Column 5, lines 19 to 33).

<u>Differences Between The Prior Art And The Claimed Invention:</u>

Claim 12 depends from independent claim 1. Applicant submits that independent claims 1 and 13 as amended are not obvious over the cited references because the cited references, alone or in combination, do not teach or suggest, each and every limitation of claims 1 and 13, as amended.

In particular, Applicants submit DIMARIA does not teach or reasonably suggest a gate insulator layer including *a conductive path formed by the diffusion of conductive elements from the diffusive metal through the gate insulator in response to a write voltage applied to the diffusive metal*, or that *the floating gate is adapted to prevent the conductive elements from the diffusive metal from diffusing into the channel region below the at least one floating gate.*

As noted above, Applicants submit that the arrows in insulator 5 extending between electron in injectors 1 and 3 in FIG. 1 of DIMARIA illustrates the injection of electrons from the injectors 1, 3, for negative and positive Vg respectively, and not, as in the present invention, a conductive path formed by the diffusion of conductive elements from a diffusive metal in the gate 2 through the gate insulator.

Applicants also submit that, contrary to the present invention, DIMARIA teaches that the dual injectors 1, 3, and the insulator 5 disposed between these injectors are rendered conductive during deposition.

Finally, Applicants submit that DIMARIA does not teach or reasonably suggest the limitation of the floating gate adapted to prevent the conductive elements from the diffusive metal from diffusing into the channel region below the at least one floating gate. First, as noted above DIMARIA does not teach or suggest diffusion of conducting elements from the gate electrode 2, therefore there would be no reason for DIMARIA to does not teach or suggest a diffusion barrier. Second, the floating gate of the present invention is adapted to prevent the conductive elements from the diffusive metal through the selection of material of the floating gate and the size of the floating gate relative to the diffusive metal. As noted above, the floating gate comprises a metal selected from the group consisting of W, Al, Cr, TiW, and Cu,

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and as shown in FIGs. 3A, 3B, 5, 15A and 15B has a width much greater than the diffusive metal.

In contrast, DIMARIA at no point teach or suggests that the floating polysilicon gate 4 could be made of anything other than polysilicon, and clearly shows in FIG. 1 the floating polysilicon gate as being equal in size with the gate electrode 2.

Similarly, with respect to the remaining cited references, KOJIMA, NOGUCHI and NGO, Applicant submits they at no point teach or reasonably suggest a memory cell wherein the gate insulator layer includes *a conductive path formed by the diffusion of conductive elements from the diffusive metal through the gate insulator in response to a write voltage applied to the diffusive metal*, or that *the floating gate is adapted to prevent the conductive elements from the diffusive metal from diffusing into the channel region below the at least one floating gate.*

KOJIMA does not mention diffusion of conductive elements from gate electrodes at all much less describe such diffusion as desirable to form a conductive path. Moreover, KOJIMA appears to show the in several figures, including FIGs. 9, 10 and 12, that the floating gates are much smaller than the gate electrodes and therefore would not serve effectively as diffusion barriers.

NOGUCHI likewise does not teach or suggest diffusion of conductive elements from gate electrodes to form a conductive path to the floating gate. Neither is there any mention in NOGUCHI of diffusion barriers and teaching or suggestion of the floating gate being adapted to serve as such.

NGO not only fails to teach or suggest conductive path formed by the diffusion of conductive through the gate insulator, or that the floating gate is a diffusion barrier, NGO

actually teaches away from the claimed invention by teaching diffusion into the dielectric (insulator) as very undesirable problem to be overcome. (Col. 6, line 61, to col. 7, line 19).

Accordingly, Applicants submit that the cited references, alone or in combination, do not teach or suggest, each and every limitation of claims 1 and 13, as amended, and respectfully requests the rejection be withdrawn, and that claims 12 and 13 and claims 14-20 which are dependent therefrom be allowed.

CONCLUSION

Applicant respectfully requests reconsideration of the above-identified application in view of the preceding remarks and exhibits.

In the event that the Examiner identifies any other issues that would preclude issuing a Notice of Allowance, the courtesy of a telephone call to the undersigned attorney would be appreciated.

The Commissioner is authorized to charge any additional fees, such as fees for extension of time and claims added herein but not otherwise paid for, to Deposit Account No. 08-2025 (Order No. HP 10015160-1).

Respectfully submitted,

By: ______________________
William E. Nuttle, Reg. No. 42,943

DORSEY & WHITNEY LLP
4 Embarcadero Center, Suite 3400
San Francisco, CA 94111-4187
Telephone: (650) 494-8700
Facsimile: (650) 494-8771